AMENDMENTS TO THE SPECIFICATION

Please replace paragraph beginning at page 7, line 18, with the following amended paragraph:

The arbiter ~~201~~ 206 may be coupled to each of the buses shown in Fig. 2. The request and grant lines may be incorporated into the buses as well or may be separately coupled to the arbiter. In fact, the arbiter, rather than being separate as shown, may in fact reside in one or more of the processors or memories, or be distributed among the processors and memories in a manner described further herein.

Please replace paragraph beginning at page 7, line 23, with the following amended paragraph:

Assuming a central arbitration scheme utilizing arbiter ~~201~~ 206, processor P0 requests transaction T0 for memory M0 from the arbiter, processor P1 requests transactions T0 and T2 for memories M0 and M2, respectively. Processor P2 requests transactions T0, T1 and T2 to memories M0, M1 and M2, respectively. As with the switch embodiment described previously, the arbiter gives the highest priority to processor P0 since that processor has the fewest requests. After P0 is granted its T0 request, P1 has one request pending and P2 has two requests pending, since M0 has already been allocated. Thus, P1 is granted its T2 request since it has higher priority (only one request) and finally P2 is granted its T1 request. Thus, the arbiter grants P0 its T0 request, P1 its T2 request and P2 its T1 request, thus maximizing utilization of buses 200.